



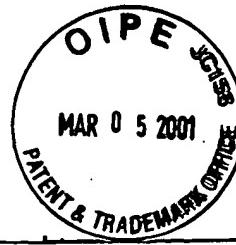
In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked-up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

RECEIVED  
MAR - 8 2001  
TECHNOLOGY CENTER 2800

CLAIMS



1. (Amended) Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions, the high K substantially crystalline material being received over the high K substantially amorphous material.

*A1*  
Cancel claims 2 and 3.

RECEIVED  
MAR 3 2001  
TECHNOLOGY CENTER 2800

4. The integrated circuitry of claim 1 wherein at least one of the first and second electrodes comprises elemental metal, metal alloy, conductive metal oxides, or mixtures thereof.

5. The integrated circuitry of claim 1 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

6. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

7. The integrated circuitry of claim 6 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode.

8. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrodes and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes.

9. The integrated circuitry of claim 1 wherein the high K capacitor dielectric region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

10. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous, and the high K substantially crystalline material layer is at least 98% crystalline.

11. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially crystalline material layer being received between the semiconductor substrate and the high K substantially amorphous material layer.

12. The integrated circuitry of claim 11 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

13. The integrated circuitry of claim 11 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

14. The integrated circuitry of claim 11 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

15. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.

16. The integrated circuitry of claim 15 wherein the semiconductor substrate comprising bulk monocrystalline silicon.

Cancel claims 17-55.